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TITLE

METHOD FOR CPU POWER MANAGEMENT AND BUS OPTIMIZATION

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates in general to a method for CPU power management and bus optimization. In particular, the present invention relates to a method for I/O link protocol technology and power management on AMD K8 platform.

Description of the Related Art

Legacy I/O bus architectures are widely used in embedded systems because they are low cost and easily implemented using established software and hardware standards. These busses, however, top out at 66MHz or so. Recently, processors operating at 500MHz and 1GHz and up clock frequencies need a faster alternative to these low bandwidth busses.

Lightning data transport (LDT) I/O bus, sometimes referred to hyper-transport (HT) I/O bus, delivers the high bandwidth needed for high performance applications in networking, communications and other embedded applications in a flexible, extensible and easily implemented bus structure. A scalable solution, the LDT I/O bus is capable of providing bandwidth for next generation processors and communications systems. A multivendor standard that is easily implemented, the LDT solution provides a broad selection of bus widths and speeds meeting the power, space and cost requirements of a wide range of embedded systems from low cost desktop workstations to digital consumer applications, communication systems, and networking equipment.

The optimization of LDT I/O bus is achieved through disconnection and reconnection of the LDT I/O bus enabling the LDT I/O bus to perform at desired bandwidth and operating frequency.

FIG. 1 is a flowchart of the optimization of bandwidth and operating frequency of conventional LDT I/O bus. First, LDT bus is initialized by basic input/output system (BIOS) (S1), such as by setting the optimized bandwidth and operating frequency of LDT bus connected between CPU and the Northbridge after booting. For example, the bandwidth of the LDT bus may be initialized as 8-bit, but can be changed to 16-bit after optimization. The operating frequency of the LDT bus may be initialized as 200MHz, but can be changed to 400MHz, 600MHz or 800MHz after optimization. Here, the optimized bandwidth and operating frequency of LDT bus are set by BIOS. Next, power management resisters of CPU and the chipset comprising a Northbridge and a Southbridge are initialized by BIOS to set the related power setting (S2). Next, an auto-resume timer in the Southbridge is initialized for calculating an elapsed time value (S3). Next, BIOS issues a read request to a Southbridge power management I/O (PMIO) offset 15h for asserting a signal LDTSTOP# (S4). Here, the asserting of the signal LDTSTOP# transforms a high level signal LDTSTOP# to a low level signal LDTSTOP#. The LDT bus connected between CPU and the Northbridge is disconnected when the signal LDTSTOP# is asserted.

Next, the Southbridge de-asserts the signal LDTSTOP# when the elapsed time value of the timer initialized in step S3 reaches a predetermined value (S5). Here, the de-asserting of the signal LDTSTOP# transforms a low level signal LDTSTOP# to a high level signal LDTSTOP#. Thus, the LDT bus connected between CPU and the Northbridge is reconnected when the signal LDTSTOP# is

de-asserted (S6). Therefore, the LDT bus operates at optimized bandwidth and operating frequency set in BIOS. Thus, optimization of bandwidth and operating frequency of LDT bus is completed.

Power management is another important boot process in computer systems. FIG. 2 shows a conventional power management process. First, power management resisters of CPU and the chipset comprising the Northbridge and the Southbridge are initialized by BIOS to set the related power setting (S21). Next, maximum operating frequency and voltage of CPU are obtained from the register FIDVID_STATUS of CPU and stored in the register FIDVID_CTL of CPU by BIOS (S22). Next, an auto-resume timer in the Southbridge is initialized for calculating an elapsed time value (S23). Next, CPU outputs a FID/VID change message to the Southbridge and the signal LDTSTOP# is asserted when the Southbridge receives the FID/VID change message (S24). Here, the asserting of the signal LDTSTOP# also transforms a high level signal LDTSTOP# to a low level signal LDTSTOP#. The LDT bus connected between CPU and the Northbridge is disconnected when the signal LDTSTOP# is asserted. Next, operating frequency and voltage of CPU are changed according to the setting in FIDVID_CTL register (S25). Next, the Southbridge de-asserts the signal LDTSTOP# when the elapsed time value of the timer initialized in step S24 reaches another predetermined value (S26). Here, the de-asserting of the signal LDTSTOP# transforms a low level signal LDTSTOP# to a high level signal LDTSTOP#. Thus, the LDT bus connected between CPU and the Northbridge is reconnected when the signal LDTSTOP# is de-asserted (S27). Therefore, CPU operates at the adjusted operating frequency with the adjusted operating voltage. Thus, power management of CPU is achieved.

Power management of CPU and LDT bus optimization described are performed independently during boot. However, the disconnection and reconnection of LDT bus are performed in both processes. The repeated hardware operation causes booting delay and complicates of boot process.

SUMMARY OF THE INVENTION

The object of the present invention is thus to provide a method for CPU power management and bus optimization combining the processes of power management of CPU with bus optimization into a single flow, avoiding repeated disconnection and reconnection of the LDT bus, thereby improving boot efficiency.

To achieve the above-mentioned object, the present invention provides a method for CPU power management and bus optimization. First, the bus operates at an initial bus bandwidth and an initial bus frequency. Next, power management settings of the CPU, the Northbridge and the Southbridge are initialized, such that the CPU operates at a CPU operating frequency with a CPU operating voltage. Next, a CPU operating frequency and voltage adjustment is output to the Southbridge. Next, a bus disconnection signal is output by the Southbridge to disconnect the CPU and the Northbridge, and a timer for calculating an elapsed time value is initialized. Next, the CPU operating frequency and the CPU operating voltage are adjusted according to the CPU operating frequency and voltage adjustment. Next, a bus connection signal is output by the Southbridge when the elapsed time value reaches a predetermined value. Next, the CPU and the Northbridge are reconnected by the bus according to the bus connection signal. Finally, the bus operates at the bus

operating bandwidth and the bus operating frequency, and the CPU operates at the adjusted CPU operating frequency with the adjusted CPU operating voltage according to the CPU operating frequency and voltage adjustment.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings, given by way of illustration only and thus not intended to be limitative of the present invention.

FIG. 1 is a flowchart of optimization of bandwidth and operating frequency of conventional LDT I/O bus.

FIG. 2 shows a conventional power management process.

FIG. 3 is a schematic diagram of a computer system comprising LDT bus.

FIG. 4 is a flowchart of LDT bus optimization and CPU power management according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 3 shows a schematic diagram of a computer system comprising an LDT bus. As shown in the figure, LDT bus 12 is connected between CPU 10 and the Northbridge 14. Here, CPU 10 is an AMD K8 CPU, although the invention encompasses a wide range of CPU types, makes and models. Another bus 16 is connected between the Northbridge 14 and the Southbridge 18. LDT bus 12, connected between CPU 10 and the Northbridge 14, is disconnected and reconnected during power management of CPU and LDT bus optimization. Disconnection and reconnection of LDT bus 12 are performed according to the voltage level of the signal LDTSTOP# output by the Southbridge 18. The Southbridge 18 asserts the

signal LDTSTOP# and outputs the asserted signal LDTSTOP#. LDT bus 12 is disconnected when both CPU 10 and the Northbridge 14 receive the asserted signal LDTSTOP#. Next, the timer 19 of the Southbridge 18 begins to calculate an elapsed time value. The Southbridge 18 de-asserts the signal LDTSTOP# when the elapsed time value of the timer 19 reaches a predetermined value. LDT bus 12 is reconnected when both CPU 10 and the Northbridge 14 receive the de-asserted signal LDTSTOP#. Thus, LDT bus operates at another operating frequency and bandwidth, and CPU operates at a different operating voltage and frequency.

FIG. 4 is a flowchart of the LDT bus optimization and CPU power management according to the present invention. According to the present invention, LDT bus optimization is completed during CPU power management. Here, CPU power management is carried out by "AMD PowerNow!" technology.

AMD PowerNow! technology is an advanced, second-generation power-management feature that reduces the overall power consumed by the processor through control of voltage and frequency. This power-saving technology is designed to be dynamic and flexible by enabling instant, on-the-fly, and independent control of both the voltage and frequency. AMD PowerNow! technology enables reduced power consumption with performance on demand for power-sensitive embedded applications. For notebooks, operating voltage and frequency of CPU are decreased to save power, increase battery life, and decrease system temperature when CPU loading is low. The operating voltage and frequency of CPU are both increased as more operating steps are required. The CPU loading is detected by the operating system, whereby operating voltage and frequency of which is adjusted. All possible settings of operating voltage and frequency of the CPU are stored in BIOS

power management settings and are adjustable by users. The settings of operating frequency and voltage correspond to CPU type.

In FIG. 4, first, LDT bus is initialized by basic input/output system (BIOS) (S31), such as by setting the optimized bandwidth and operating frequency of LDT bus connected between CPU and the Northbridge after booting. For example, the bandwidth of the LDT bus may be initialized as 8-bit, but can be changed to 16-bit after optimization. The operating frequency of the LDT bus may be initialized as 200MHz, but can be changed to 400MHz, 600MHz or 800MHz after optimization. Here, the optimized bandwidth and operating frequency of LDT bus are set by BIOS. Next, power management resisters of CPU and the chipset comprising the Northbridge and the Southbridge are initialized by BIOS to set the related power setting (S32). Thus, the CPU operates at an initial frequency and voltage, and CPU loading is detected.

Next, maximum operating frequency and voltage of CPU are obtained from register FIDVID_STATUS of CPU and stored to a register FIDVID_CTL of CPU by BIOS (S33). Next, an auto-resume timer in the Southbridge is initialized for calculating an elapsed time value (S34). Next, CPU outputs a FID/VID change message to the Southbridge according to the maximum operating frequency and voltage and the signal LDTSTOP# is asserted when the Southbridge receives the FID/VID change message (S35). Thus, operating voltage and frequency of the CPU are changed according to the FID/VID change message before LDT bus is reconnected. Here, the adjusted operating voltage and operating frequency of CPU must respectively be lower than or equal to the maximum operating frequency and maximum operating voltage.

Here, the asserting of the signal LDTSTOP# also transforms a high level signal LDTSTOP# to a low level signal LDTSTOP#. The LDT bus connected between CPU and the Northbridge is disconnected when the signal LDTSTOP# is asserted. Next, the operating frequency and voltage of CPU are changed according to the setting in FIDVID_CTL register (S36). Next, the Southbridge de-asserts the signal LDTSTOP# when the elapsed time value of the timer initialized in step S34 reaches another predetermined value (S37). Here, the de-asserting of the signal LDTSTOP# transforms a low level signal LDTSTOP# to a high level signal LDTSTOP#. Thus, the LDT bus connected between CPU and the Northbridge is reconnected when the signal LDTSTOP# is de-asserted (S38). Simultaneously, the LDT bus operates at the optimized bandwidth and operating frequency preset in BIOS in step S31. Thus, optimization of bandwidth and operating frequency of LDT bus, and power management of CPU, are simultaneously achieved.

The method for CPU power management and bus optimization according to the present invention combines conventional power management of CPU with conventional LDT bus optimization, which are performed independently during boot. Thus, logic operation and hardware setting time of CPU power management and bus optimization are decreased. In addition, while conventional power management of CPU and conventional LDT bus optimization comprise 13 steps, only 8 steps are required to complete the operations according to the present invention. Thus, boot efficiency is significantly improved.

The foregoing description of the preferred embodiments of this invention has been presented for purposes of illustration and description. Obvious modifications or variations are

possible in light of the above teaching. The embodiments were chosen and described to provide the best illustration of the principles of this invention and its practical application to thereby enable those skilled in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. All such modifications and variations are within the scope of the present invention as determined by the appended claims when interpreted in accordance with the breadth to which they are fairly, legally, and equitably entitled.